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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/067,153	02/04/2002	Il-Young Sohn	8836-106 DIV	7320

7590 05/18/2005

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EXAMINER

JERABEK, KELLY L

ART UNIT	PAPER NUMBER
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2612

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/067,153

Applicant(s)

SOHN, IL-YOUNG

Examiner

Kelly L. Jerabek

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Preliminary Amendment filed 2/4/2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 5,6 and 9-16 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 5 and 6 is/are allowed.
- 6) ☒ Claim(s) 9-16 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 9-16 rejected under 35 U.S.C. 103(a) as being unpatentable over the Applicant's Admitted Prior Art in view of Mizuno et al. US 5,912,463.

Re claim 13, the Applicant's specification details a CMOS active pixel sensor as Admitted Prior Art. The CMOS active pixel sensor includes a reset step wherein a reset transistor (14) resets a voltage level of a photodiode (12), an image integration step for applying light energy to the photodiode (12), and a readout step for reading a pixel voltage of the CMOS active pixel sensor by sensing the voltage of the photodiode (12) after light energy is applied (Specification: page 1, line 13 – page 3, line 11; figs. 1-2).

The Applicant's Admitted Prior Art also states that during a non-exposure time for light incidence the pixel voltage is lowered by a voltage corresponding to the dark current of the photodiode (12) (Specification: page 3, lines 1-16). Although the Applicant's Admitted Prior Art discloses all of the above limitations it fails to disclose a method of compensating for a reduction in the pixel voltage caused by leakage current of the first photodiode using leakage current of a second photodiode.

Mizuno discloses in figure 3 a photodetector included in a solid-state imaging apparatus and having a first photodiode (110) adapted to generate an electric charge in response to an incident light and a second light-shielded photodiode (120) having a dark current characteristic substantially identical to that of the first photodiode (120) (col. 12, lines 28-50). The dark current value generated by the light-shielded photodiode (120) is used to subtract the dark current from the electric charge generated by the first photodiode (110). Timing generation circuit (600) includes reset signals (R1,R2) for resetting the photodiodes, integration signal (SM), subtraction signal (SB), and dark current cancel instruction signal (RM). The dark current cancel instruction signal (RM) causes a dark current canceling circuit (400) to subtract the dark current from the current flowing into the input terminal of the integrating circuit (300) (col. 13, line 23 – col. 14, line 63). Thus, a reduction in the pixel voltage caused by leakage current (dark current) of the first photodiode (110) is compensated for using leakage current (dark current) of the second photodiode (120). Therefore, it would have been obvious for one skilled in the art to have been motivated to include the teaching of using a second light-shielded photodiode to compensate for a reduction in pixel voltage due to dark current

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of a first photodiode as disclosed by Mizuno in the CMOS active pixel sensor including a dark current component as disclosed by the Applicant's Admitted Prior Art. Doing so would provide a means for extracting a dark current value of a photodiode using a light-shielded photodiode in order to determine the intensity of light accurately (Mizuno: col. 4, lines 45-60).

Re claim 14, Mizuno discloses a second photodiode (120) that is shielded from light incidence.

Re claim 15, the Applicant's Admitted Prior Art states that after a photodiode (12) is reset, the voltage of the photodiode is lowered by a voltage corresponding to dark current. Mizuno discloses a dark current cancel instruction signal (RM) that causes a dark current canceling circuit (400) to subtract the dark current from the current flowing into the input terminal of the integrating circuit (300) (col. 13, line 23 – col. 14, line 63). Therefore, implementing the Mizuno teaching of a dark current cancel instruction in the admitted prior art CMOS active pixel sensor will increase the amount of current flowing to a bit line in an amount proportional to the amount of decreased current flow to the bit line due to a decreased voltage of a light-sensing photodiode.

Re claim 16, Mizuno states that the dark current cancel instruction is performed by a dark current canceling circuit (400) that includes a transistor (410) connected to a light-shielded photodiode (120) (col. 13, lines 50-63).

Re claim 9, see claim 13.

Re claim 10, see claim 14.

Re claim 11, see claim 15.

Re claim 12, see claim 16.

Allowable Subject Matter

Claims 5-6 allowed.

The following is a statement of reasons for the indication of allowable subject matter: the prior art of record fail to anticipate or render obvious the following technical features as recited in the highlighted claims:

Referring to claims 5 and 6, the prior art fails to teach or suggest " A method of increasing voltage readout sensitivity of a CMOS active pixel sensor, said sensor including a first photodiode having leakage current flow, a first reset transistor for resetting photodiode voltage and a first sense transistor connected to said photodiode, the method comprising the steps of:

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Commonly connecting a second sense transistor at a drain...to said first sense transistor;

Commonly connecting a second reset transistor to said first reset transistor for activating both first and second reset transistors by a reset signal;

Shielding a second photodiode...and second source transistor; and

Reading out voltage upon illumination of incident light on said first photodiode by activating a select transistor connected to said first and second sense transistors".

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nakamura et al. (US 6,690,423) discloses a solid-state image pickup apparatus. The information regarding shielded photodiodes is relevant material.

Nishibe et al. (US 4,916,307) discloses a light intensity detecting circuit with dark current compensation. The information regarding shielded photodiodes is relevant material.

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Kozlowski et al. (US 6,498,331) discloses a method and apparatus for achieving uniform low dark current with CMOS photodiodes. The information regarding dark current in CMOS photodiodes is relevant material.

Afghahi (US 6,747,695) discloses an integrated CMOS imager. The information regarding dark current in CMOS photodiodes is relevant material.

Contacts


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wendy Garber can be reached on **(571) 272-7308**. The fax phone number for submitting all Official communications is 703-872-9306. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KLJ


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